IN THE CLAIMS

Listing of the claims:

1. (original) A multiphase buck converter system with peak current sharing comprising:

a first buck converter coupled to a first regulator input voltage and generating a first converter output voltage for powering a common load in response to a first ON-time pulse set to a first logic state by a first start signal and set to a second logic state by a first stop signal, wherein said first converter output voltage supplies energy to said common load directly from said first regulator input voltage when said first ON-time pulse has said first logic state and said first converter output voltage supplies stored energy from said first regulator input voltage when said first ON-time pulse has said second logic state;

a second buck converter coupled to a second regulator input voltage and generating a second converter output voltage for powering said common load in response to a second ON-time pulse set to a first logic state by a second start signal and set to a second logic state by a second stop signal, wherein said second converter output voltage supplies energy to said common load directly from said second regulator input voltage when said second ON-time pulse has said first logic state and said second converter output voltage supplies stored energy from said second regulator input voltage when said second ON-time pulse has said second logic state;

start circuitry for generating said first and second start signals in response to a regulated voltage across said common load, a reference voltage, and said first and second ON-time pulses;

first stop circuitry for generating said first stop signal in response to said first regulator input voltage and said reference voltage; and

second stop circuitry for generating said second stop signal in response to a first output current from said first converter output voltage supplied to said common load, a second output current from said second converter output voltage supplied to said common load, and said first ON-time pulse.

2. (original) The converter system of claim 1, wherein said first stop circuitry comprises:

a capacitor charged by a current from said first regulator input voltage when said first ON-time pulse has said first logic state and discharged when said first ON-time pulse has said second logic state; and

first compare circuitry for comparing said reference voltage to a capacitor voltage across said capacitor and generating said first stop signal, wherein said first stop signal has a first logic state when said capacitor voltage is greater than said reference voltage and a second logic state when said capacitor voltage is less than said reference voltage.

3. (original) The converter system of claim 2, wherein said second stop circuitry comprises:

peak circuitry for generating a peak voltage proportional to a peak value of said first output current;

first sense circuitry for generating a first sense voltage proportional to said second output current; and

second compare circuitry for comparing said first sense voltage to said peak voltage and generating said second stop signal, wherein said second stop signal has a first logic state when said first sense voltage is greater than said peak voltage and a second logic state when said first sense voltage is less than said peak voltage.

4. (original) The converter system of claim 3, wherein said first sense circuitry comprises:

a first sense resistor having a first terminal coupled to said first converter output voltage and a second terminal coupled to said common load; and

a differential amplifier having a positive input coupled to said first terminal of said first sense resistor and a negative input coupled to said second terminal of said first sense resistor, and an output generating said first sense voltage.

5. (original) The converter system of claim 3, wherein said peak circuitry comprises:

a second sense resistor having a first terminal coupled to said second converter output voltage and a second terminal coupled to said common load;

a differential amplifier having a positive input coupled to said first terminal of said second sense resistor and a negative input coupled to said second terminal of said second sense resistor, and an output generating said second sense voltage; and

a sampling circuit for tracking said second sense voltage when said first ON-time pulse has said first logic state and holding a value of said second sense voltage as said peak voltage when said ON-time pulse has said second logic state.

6. (original) The converter system of claim 3, wherein said start circuitry comprises:

a compare circuit for comparing said regulated voltage across said common load to said reference voltage and generating a gate signal having a first logic state when said reference voltage is greater than said regulated voltage and a second logic state when said reference voltage is less than said regulated voltage;

a first select circuit for generating said first start signal in response to said first ON-time pulse, said gate signal, said second start signal, and an initialization signal; and

a second select circuit for generating said second start signal in response to said second ON-time pulse, said gate signal, said first start signal, and said initialization signal.

7. (original) The converter system of claim 5, wherein said sampling circuit comprises:

a capacitor having a first terminal coupled to ground and a second terminal; and

an electronic switch for coupling said second sense voltage to said first terminal of said capacitor when said first ON-time pulse has said first logic state, said capacitor holding said value of said sense voltage as said peak voltage when said first ON-time pulse has said second logic state.

8. (original) The converter system of claim 6, wherein said first select circuit comprises:

a compare logic circuit for generating a compare logic signal in response to said regulated voltage across said common load, said reference voltage, and said initialization signal;

an initialization pulse circuit for generating an initialization pulse in response to said initialization signal and said compare logic signal;

a first logic circuit for generating said first start signal in response to said first ON-time pulse, said initialization pulse, and said second start signal; and

a second logic circuit for generating said second start signal in response to said second ON-time pulse, said initialization pulse, and said first start signal.

9. (original) The converter system of claim 8, wherein said compare logic circuit comprises:

a comparator for comparing said reference voltage to said regulated voltage across said common load and generating a compare output signal having a first logic state when said reference voltage is greater than said regulated voltage across said common load and a second logic state when said regulated voltage across said common load is greater than said reference voltage; and

a logic gate generating said compare logic signal as logic combination of said compare output signal and said initialization signal.

10. (original) The converter system of claim 9, wherein said initialization pulse circuit comprises:

a logic gate generating a start converter signal as a logic combination of said initialization signal and said compare logic signal; and

a pulse circuit generating said initialization pulse in response to a logic transition of said start converter signal.

11. (original) The converter system of claim 10, wherein said first logic circuit comprises:

a flip-flop having an output, an inverted output, a data input, a set input, a reset input, and a clock input, wherein said set input is coupled to said initialization pulse, said clock input is coupled to said second start signal, and said inverted output is coupled to said data input;

a positive pulse circuit having an input coupled to said first start signal and an output coupled to said reset input of said flip-flop and generating a reset pulse in response to a logic transition of said first start signal;

an inverted pulse circuit having an input coupled to said first ON-time pulse and an output generating an inverted pulse, wherein said inverted pulse circuit generates said inverted pulse in response to a logic transition of said first ON-time pulse;

a third logic circuit having a first input coupled to said compare logic signal, a second input, a third input coupled to said output of said inverted pulse circuit, and generating said first start signal; and

a delay circuit having an input coupled to said output of said flip-flop and a delay output coupled to said second input of said third logic circuit, wherein said delay circuit selectively delays a logic transition of said delay output.

12. (original) The converter system of claim 10, wherein said second logic circuit comprises:

a positive pulse circuit having an input coupled to said second start signal and an output generating a reset pulse on a logic transition of said second start signal;

a logic gate having a first input coupled to said initialization pulse, a second input coupled to said output of said positive pulse circuit, and an output generating a gated reset pulse as a logic combination of said initialization pulse and said output of said positive pulse circuit;

a flip-flop having an output, an inverted output, a data input, a reset input, and a clock input, wherein said reset input is coupled to said output of said logic gate, said clock input is coupled to said first start signal, and said inverted output is coupled to said data input;

an inverted pulse circuit having an input coupled to said first ON-time pulse and an output generating an inverted pulse, wherein said inverted pulse circuit generates said inverted pulse in response to a logic transition of said first ON-time pulse;

a third logic circuit having a first input coupled to said compare logic signal, a second input, a third input coupled to said output of said inverted pulse circuit, and generating said second start signal; and

a delay circuit having an input coupled to said output of said flip-flop and a delay output coupled to said second input of said third logic circuit, wherein said delay circuit delays a logic transition of said delay output.

13. (original) The converter system of claim 4, wherein said differential amplifier is a transconductance amplifier for converting a voltage across said first sense resistor to a first sense current coupled to a first resistor thereby generating said first sense voltage across said first resistor.

14. (original) The converter system of claim 5, wherein said differential amplifier is a transconductance amplifier for converting a voltage across said second sense resistor to a second sense current coupled to a second resistor thereby generating said second sense voltage across said second resistor.

15. (original) The converter system of claim 1, wherein said first ON-time pulse is generated as an output of a latch set by a first logic state of said first start signal and reset by a first logic state of said first stop signal.

16. (original) The converter system of claim 1, wherein said second ON-time pulse is generated as an output of a latch set by a first logic state of said second start signal and reset by a first logic state of said second stop signal.

17. (original) A computer system comprising:

one or more central processing units (CPUs);

a memory for storing instructions and data for said CPUs;

a power system for supplying power to said computer system;

a first buck converter coupled to a first regulator input voltage and generating a first converter output voltage for powering a common load in response to a first ON-time pulse set to a first logic state by a first start signal and set to a second logic state by a first stop signal, wherein said first converter output voltage supplies energy to said common load directly from said first regulator input voltage when said first ON-time pulse has said first logic state and said first converter output voltage supplies stored energy from said first regulator input voltage when said first ON-time pulse has said second logic state;

a second buck converter coupled to a second regulator input voltage and generating a second converter output voltage coupled for powering said common load in response to a second ON-time pulse set to a first logic state by a second start signal and set to a second logic state by a second stop signal, wherein said second converter output voltage supplies energy to said common load directly from said second regulator input voltage when said second ON-time pulse has said first logic state and said second converter output voltage supplies stored energy from said second regulator input voltage when said second ON-time pulse has said second logic state;

start circuitry for generating said first and second start signals in response to a regulated voltage across said common load, a reference voltage, and said first and second ON-time pulses;

first stop circuitry for generating said first stop signal in response to said first regulator input voltage and said reference voltage; and

second stop circuitry for generating said second stop signal in response to a first output current from said first converter output voltage supplied to said common load, a second output current from said second converter output voltage supplied to said common load, and said first ON-time pulse.

18. (original) The system of claim 17, wherein said first stop circuitry comprises:

a capacitor charged by a current from said first regulator input voltage when said first ON-time pulse has said first logic state and discharged when said first ON-time pulse has said second logic state; and

first compare circuitry for comparing said reference voltage to a capacitor voltage across said capacitor and generating said first stop signal, wherein said first stop signal has a first logic state when said capacitor voltage is greater than said reference voltage and a second logic state when said capacitor voltage is less than said reference voltage.

19. (original) The system of claim 18, wherein said second stop circuitry comprises:

peak circuitry for generating a peak voltage proportional to a peak value of said first output current;

first sense circuitry for generating a first sense voltage proportional to said second output current; and

second compare circuitry for comparing said first sense voltage to said peak voltage and generating said second stop signal, wherein said second stop signal has a first logic state when said first sense voltage is greater than said peak voltage and a second logic state when said first sense voltage is less than said peak voltage.

20. (original) The system of claim 19, wherein said first sense circuitry comprises:

a first sense resistor having a first terminal coupled to said first converter output voltage and a second terminal coupled to said common load; and

a differential amplifier having a positive input coupled to said first terminal of said first sense resistor and a negative input coupled to said second terminal of said first sense resistor, and an output generating said first sense voltage.

21. (original) The system of claim 19, wherein said peak circuitry comprises:

a second sense resistor having a first terminal coupled to said second converter output voltage and a second terminal coupled to said common load;

a differential amplifier having a positive input coupled to said first terminal of said second sense resistor and a negative input coupled to said second terminal of said second sense resistor, and an output generating said second sense voltage; and

a sampling circuit for tracking said second sense voltage when said first ON-time pulse has said first logic state and holding a value of said second sense voltage as said peak voltage when said ON-time pulse has said second logic state.

22. (original) The system of claim 19, wherein said start circuitry comprises:

a compare circuit for comparing said regulated voltage across said common load to said reference voltage and generating a gate signal having a first logic state when said reference voltage is greater than said regulated voltage and a second logic state when said reference voltage is less than said regulated voltage;

a first select circuit for generating said first start signal in response to said first ON-time pulse, said gate signal, said second start signal, and an initialization signal; and

a second select circuit for generating said second start signal in response to said second ON-time pulse, said gate signal, said first start signal, and said initialization signal.

23. (original) The system of claim 21, wherein said sampling circuit comprises:

a capacitor having a first terminal coupled to ground and a second terminal; and

an electronic switch for coupling said second sense voltage to said first terminal of said capacitor when said first ON-time pulse has said first logic state, said capacitor

holding said value of said sense voltage as said peak voltage when said first ON-time pulse has said second logic state.

24. (original) The system of claim 22, wherein said first select circuit comprises:

a compare logic circuit for generating a compare logic signal in response to said regulated voltage across said common load, said reference voltage, and said initialization signal;

an initialization pulse circuit for generating an initialization pulse in response to said initialization signal and said compare logic signal;

a first logic circuit for generating said first start signal in response to said first ON-time pulse, said initialization pulse, and said second start signal; and

a second logic circuit for generating said second start signal in response to said second ON-time pulse, said initialization pulse, and said first start signal.

25. (original) The system of claim 24, wherein said compare logic circuit comprises:

a comparator for comparing said reference voltage to said regulated voltage across said common load and generating a compare output signal having a first logic state when said reference voltage is greater than said regulated voltage across said common load and a second logic state when said regulated voltage across said common load is greater than said reference voltage; and

a logic gate generating said compare logic signal as logic combination of said compare output signal and said initialization signal.

26. (original) The system of claim 25, wherein said initialization pulse circuit comprises:

a logic gate generating a start converter signal as a logic combination of said initialization signal and said compare logic signal; and

a pulse circuit generating said initialization pulse in response to a logic transition of said start converter signal.

27. (original) The system of claim 26, wherein said first logic circuit comprises:

a flip-flop having an output, an inverted output, a data input, a set input, a reset input, and a clock input, wherein said set input is coupled to said initialization pulse, said clock input is coupled to said second start signal, and said inverted output is coupled to said data input;

a positive pulse circuit having an input coupled to said first start signal and an output coupled to said reset input of said flip-flop and generating a reset pulse in response to a logic transition of said first start signal;

an inverted pulse circuit having an input coupled to said first ON-time pulse and an output generating an inverted pulse, wherein said inverted pulse circuit generates said inverted pulse in response to a logic transition of said first ON-time pulse;

a third logic circuit having a first input coupled to said compare logic signal, a second input, a third input coupled to said output of said inverted pulse circuit, and generating said first start signal; and

a delay circuit having an input coupled to said output of said flip-flop and a delay output coupled to said second input of said third logic circuit, wherein said delay circuit selectively delays a logic transition of said delay output.

28. (original) The system of claim 26, wherein said second logic circuit comprises:

a positive pulse circuit having an input coupled to said second start signal and an output generating a reset pulse on a logic transition of said second start signal;

a logic gate having a first input coupled to said initialization pulse, a second input coupled to said output of said positive pulse circuit, and an output generating a gated reset pulse as a logic combination of said initialization pulse and said output of said positive pulse circuit;

a flip-flop having an output, an inverted output, a data input, a reset input, and a clock input, wherein said reset input is coupled to said output of said logic gate, said

clock input is coupled to said first start signal, and said inverted output is coupled to said data input;

an inverted pulse circuit having an input coupled to said first ON-time pulse and an output generating an inverted pulse, wherein said inverted pulse circuit generates said inverted pulse in response to a logic transition of said first ON-time pulse;

a third logic circuit having a first input coupled to said compare logic signal, a second input, a third input coupled to said output of said inverted pulse circuit, and generating said second start signal; and

a delay circuit having an input coupled to said output of said flip-flop and a delay output coupled to said second input of said third logic circuit, wherein said delay circuit delays a logic transition of said delay output.

29. (original) The system of claim 20, wherein said differential amplifier is a transconductance amplifier for converting a voltage across said first sense resistor to a first sense current coupled to a first resistor thereby generating said first sense voltage across said first resistor.

30. (original)The system of claim 21, wherein said differential amplifier is a transconductance amplifier for converting a voltage across said second sense resistor to a second sense current coupled to a second resistor thereby generating said second sense voltage across said second resistor.

31. (original) The system of claim 17, wherein said first ON-time pulse is generated as an output of a latch set by a first logic state of said first start signal and reset by a first logic state of said first stop signal.

32. 32. (original) The system of claim 17, wherein said second ON-time pulse is generated as an output of a latch set by a first logic state of said second start signal and reset by a first logic state of said second stop signal.